OPTICAL-GATE TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

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5   BACKGROUND OF THE INVENTION

Field of the Invention

[0001]   The invention relates in general to an optical-gate transistor and method of manufacturing the same, and more particularly to an optical-gate transistor, in which a prism-shaped, light-receiving layer is formed between a

10   source electrode and a drain electrode instead of a gate electrode, and method of manufacturing the same.

Description of the Related Art

[0002]   In the twenty-first century, information technology has moved into the terabyte era. Optoelectronic technology plays a very important role in

15   transmitting, processing, storing, and displaying terabyte information. The optoelectronic integrated circuit (OEIC) uses a type of manufacturing technology, which incorporates optical devices and electronic devices on a substrate. OEIC is a technique with high potential in optoelectronic technology because devices made in this manner have smaller volume, lower

20   cost, and higher stability during operation.

[0003]   FIG. 1 shows a cross-sectional view of an OEIC structure disclosed in U.S. patent number US 6355945.   In this configuration we see that a typical OEIC has a photodiode 12 as an optical circuit region and a metal semiconductor field effect transistor (MESFET) 14 as an electronic circuit region on a gallium-arsenic (GaAs) substrate 11.   The photodiode 12 is composed of an n-type gallium-nitride (GaN) layer 12a and a p-type GaN layer 12b, and the MESFET 14 includes a source electrode 14a, a gate electrode 14b, and a drain electrode 14c.   A conducting wire 16 connects the n-type electrode 18a of the photodiode 12 and the gate electrode 14b of the MESFET 14 to electrically couple the optical circuit region and the electronic circuit region.

[0004]   When the incident light 19 is received by the p-type GaN layer 12b of the photodiode 12, a photoelectric current is generated in the photodiode 12 and then converted to an electrical signal, which provides voltage for the gate electrode 14b via the conducting wire 16.   Therefore, the OEIC can be effectively used as a photoelectric switch when bias voltage is applied to the source electrode 14a and the drain electrode 14c.

[0005]   In practical applications, using thermal diffusion or an iron implantation method, an n-type silicone substrate 13, a p-type source-electrode region 15, and a p-type drain-electrode region 17 are sequentially formed on a part of the GaAs substrate 11.   Afterwards, a source electrode 14a, a gate electrode 14b, and a drain electrode 14c are formed by a photolithography and etching method to complete the process of

manufacturing MESFET 14. Subsequently, an n-type GaN layer 12a and a p-type GaN layer 12b are successively formed on another part of the GaAs substrate 11. An n-type electrode 18a and a p-type electrode 18b are further formed by a photolithography and etching method to complete the process of fabricating the photodiode 12. Due to the large lattice mismatch between the GaN layer 12a and the GaAs substrate 11, lattice defects are easily generated as the GaN layer 12a is deposited. For this reason, a zinc-oxide (ZnO) buffer layer 10 is deposited on the GaAs substrate before the GaN layer 12a. Since the lattice mismatch between the ZnO material and the GaAs substrate 11 is relatively low, a better GaN layer 12a can be formed on the GaAs substrate 11.

[0006] However, as shown in FIG. 1, the typical OEIC uses a photodiode 12 for receiving the incident light 19, which is then converted to an electric signal for controlling the gate electrode 14b of MESFET 14. This procedure of manufacturing a photodiode for receiving the incident light in order to control the MESFET 14 is unnecessary though, since the incident light can be received directly by the OEIC-designed MESFET. This prevents waste of accessible space in the integrated circuit and reduces fabrication costs.

[0007] Moreover, the photoelectric current generated by the incident light 19 and received by the photodiode 12 will be unstable, thereby providing unstable voltage for the gate electrode of the MESFET 14. In addition, the gate electrode voltage caused by the photoelectric current has to be higher than a threshold voltage to generate a drain current. As a result, the

sensitivity of the OEIC device being controlled by the illumination will be reduced.

[0008]   Furthermore, as shown in FIG. 1, the conductivity of the MESFET 14 is increased by the doped silicone substrate 13 under the gate electrode 14b, but the impurities doped in substrate 13 will also block electrons from moving between the source and the drain electrodes, thereby lowering the electron mobility in the transistor.   As OEIC applications tend to develop devices of high gain, high power, and high frequency, the issue mentioned above causes considerable restrictions.   A high electron mobility transistor (HEMT) was invented to solve the issue of hetero-junction between two GaN-group materials with different band gaps.   A narrow potential well is generated at the interface of the two GaN-group materials within the band-gap offset, where the electrons can move at a high speed without obstacles, thereby forming a two-dimensional electron gas (2DEG).   This can be applied to devices using higher frequency and higher power.   However, the drain current of the HEMT transistor is still controlled by the gate electrode, and the 2DEG effect has not yet been applied to the design of OEIC devices.

SUMMARY OF THE INVENTION

[0009]   It is therefore an objective of the invention to provide an optical-gate transistor by designing a prism-shaped, light-receiving layer between the source and drain electrodes so that the incident light can be directly received by the transistor and then focused to induce a 2DEG at the hetero-junction

interface between two GaN-group materials, thereby increasing the sensitivity of the transistor being controlled by illumination and improving the power and performance of the optical-gate transistor.

[0010]   The invention achieves the above-identified objectives by providing

5   a method of manufacturing an optical-gate transistor as described below.

[0011]   A silicone substrate is formed first, and a boron-phosphide (BP) buffer layer is then formed by a halide vapor phase epitaxy.   Afterwards, a first aluminum-nitride (AlN) layer, a GaN layer, and an n-type AlN layer are successively formed on the buffer layer by metal organic chemical vapor

10   deposition.   A second AlN layer is continuously formed by metal organic chemical vapor deposition.   A source-electrode region and a drain-electrode region are then formed by a photolithography and etching method. Subsequently, the second AlN layer is etched to form a prism-shaped, light-receiving layer.   Source and drain electrodes are formed last.   The

15   incident light is focused by the prism-shaped, light-receiving layer, which further induces a photoelectric current in the n-type AlN layer.   The induced electrons fall into the adjacent GaN layer to form a high-speed 2DEG.   In this way, the power and performance of the optical-gate transistor can be enhanced.

20   [0012]   The invention achieves the above-identified objectives by providing an optical-gate transistor structure.   The transistor includes a silicone substrate, a BP buffer layer formed on the substrate, a first AlN layer formed

on the buffer layer, a GaN layer formed on the first AIN layer, a source electrode, an n-type AIN layer, and a drain electrode, which are formed on the GaN layer, and a prism-shaped, light-receiving layer formed on the n-type AIN layer. The n-type AIN layer is positioned between the source and drain electrodes. The prism-shaped, light-receiving layer can focus the incident light, and thus improve the sensitivity of the transistor being controlled by illumination.

[0013]   Other objectives, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]   FIG. 1 (Prior Art) is a cross-sectional view of a typical OEIC structure;

[0015]   FIGS. 2A to 2D illustrate the manufacturing steps for an optical-gate transistor according to a preferred embodiment of the invention;

[0016]   FIG. 2E is a schematic view of an incident light focused by the prism-shaped, light-receiving layer in FIG. 2D;

[0017]   FIG. 3A and FIG. 3B are other steps in manufacturing the prism-shaped, light-receiving layer according to a preferred embodiment of

the invention;

[0018]   FIGS. 4A to 4C are steps for forming multiple-gate electrodes and prism-shaped, light-receiving layers according to a preferred embodiment of the invention; and

5   [0019]   FIGS. 4D to 4F are additional steps for forming multiple-gate electrodes and prism-shaped, light-receiving layers in FIG. 4C.

DETAILED DESCRIPTION OF THE INVENTION

[0020]   As described above, in order to form a prism-shaped, light-receiving layer between the source electrode and the drain electrode of the transistor,

10   the feature of the invention is that a BP buffer layer is formed on the substrate first and the GaN-group materials are then deposited so that the GaN-group layers will have a cubic lattice.   The cubic lattice has lattice surfaces <100> and <111>, and thus the prism-shaped, light-receiving layer can be easily formed by epitaxy or the etching method.   Therefore, the sensitivity of the

15   transistor being controlled by illumination is improved according to the method of the invention .

[0021]   Referring to FIG. 2A, in order to form GaN-group layers with a cubic lattice, a BP buffer layer 202 is formed on the lattice surface <100> of a silicone substrate 200.   An AlN layer 204 is formed afterwards.   The buffer

20   layer 202 is formed by a halide vapor phase epitaxy as follows.   The silicone substrate 200 is heated to 900□ in a carrier gas H_2.   Boron-chloride (BCl)

and phosphorous-chloride (PCl), or BCl and hydrogen-phosphide (HP), are used as precursors. Low-temperature BP epitaxy at about 300□ is first conducted until the BP layer is deposited to a thickness of 400 nm, and then the BP layer is deposited continuously at about 1000□ for sixty minutes until it

5   reaches a total thickness of 4560 nm.

[0022]   In addition, the AlN layer 204 is used as a method of avoiding line defects generated by a mismatch between the silicone substrate 200 and the buffer layer 202, and offsetting strain in the semiconductor layer deposited afterwards to form a better deposition structure. The AlN layer 204 can be

10   formed by a metal organic chemical vapor deposition (MOCVD) process as follows. Methyl hydrazine (MMH) and Trimethylaluminum (TMA) are used as precursors. A hydrogen gas and a nitrogen gas are supplied first, and then MMH is supplied when the temperature range reaches 350□ to 500□. After three minutes, TMA is then supplied for twenty minutes. Subsequently, the

15   TMA supply is stopped, and the chamber is heated to 800□ after five minutes. During this time, MMH is continuously supplied. Afterwards, a second round of TMA is supplied at the same temperature for sixty minutes, as well as MMH. Lastly, the TMA and MMH supply is stopped, and the temperature is maintained for thirty minutes. When the temperature is lowered to room

20   temperature, the AlN epitaxy process is complete. The AlN layer 204 can be any GaN-group material $Al_x In_y Ga_z N$ where $0< x+y+z <1$.

[0023]   Referring to FIG. 2B, subsequently, a GaN layer 206, an n-type AlN layer 208, and an AlN layer 210 are successively formed on the AlN layer 204.

The epitaxy of these three layers can be conducted by the same method used for the AlN layer 204 mentioned above, but for the GaN layer 206, MMH and Trimethylgallium (TMG) are used as precursors. The n-type AlN layer 208 is doped with a silicone impurity by high-temperature thermal diffusion or iron

5   implantation. The n-type AlN layer 208 is used to supply more free electrons as induced by illumination; the GaN layer 206 is used to separate these free electrons from impurities in the GaN layer 208 to improve electron mobility; while the AlN layer 210 is used to form a light-receiving layer. The GaN layer 206, the n-type AlN layer 208, and the AlN layer 210 can be any GaN-group

10   material $Al_x In_y Ga_z N$ where $0 < x+y+z < 1$.

[0024]   Afterwards, a source-electrode region 212 and a drain-electrode region 214 are formed by a photolithography and etching method as shown in FIG. 2C. Lastly, a prism-shaped, light-receiving layer 216 is formed by an anisotropic etching method, such as wet etching using potassium hydroxide

15   (KOH) or hydrogen-fluoride (HF), and a source electrode 212a and a drain electrode 214a are then formed to complete the fabrication of an optical-gate transistor.

[0025]   The feature of the invention lies in that the AlN layer 210 formed above will have a cubic lattice structure with lattice surfaces <100> and <111>,

20   which is different from a hexagonal GaN-group layer that is typically formed using silicon carbide (SiC) or sapphire as a substrate. When the anisotropic etching is conducted, since the etching speed on the surface <100> is lower than that on the surface <111>, the AlN layer 210 can be etched into a

prism-shaped, light-receiving layer 216 as shown in FIG. 2D. When an

incident light 218 enters the transparent prism-shaped, light-receiving layer

216 from various angles, the incident light 218 will be refracted and focused

onto the n-type AlN layer 208 positioned under the layer 216 as shown in FIG.

5   2E. Therefore, more free electrons will be induced by illumination, and the

sensitivity of the transistor being controlled by illumination will be improved.

[0026] Another key point of the invention is that at the hetero-junction

interface between the GaN layer 206 and the n-type AlN layer 208, a narrow

potential well will be formed by the different band gaps between these two

10   layers. Stimulated free electrons in the wide band-gap n-type AlN layer 208

will fall into the potential well in the narrow band-gap GaN layer 206.

Therefore, as the bias voltage is applied to the source electrode 212a and the

drain electrode 214a, a high-speed 2DEG 220 will be formed in the GaN layer

206 near the interface with the n-type AlN layer 208, and its electron mobility

15   is larger than 2000 cm^2/V·s. As a result, the transistor in the invention,

requiring no gate-electrode bias, can be operated as a switch or an amplifier

controlled by illumination, and applied to high-power, high-performance

devices.

[0027] As mentioned above, the n-type AlN layer 208 can also be a p-type

20   AlN layer, which can form a two-dimensional hole gas (2DHG) resulting in a

high-mobility conducting effect. Therefore, it does not depart from the spirit

of the invention.

[0028]   Referring to FIG. 3A, in the procedure for forming the prism-shaped, light-receiving layer 216 mentioned above, a source-electrode region 310 and a drain-electrode region 312 can also be formed first after the n-type AIN layer is formed.   Subsequently, silicone-dioxide is used as a mask to cover the source-electrode region 310 and the drain-electrode region 312.   Then an AIN selectivity epitaxy is conducted on the n-type AIN layer 208 to form a prism-shaped, light-receiving layer 314.   In the final step, a source electrode 312 and a drain electrode 314 are formed to complete the optical-gate transistor fabrication as shown in FIG. 3B.   In the selectivity epitaxy, because the AIN layer deposited according to the invention has lattice surfaces <100> and <111>, the speed of the lattice deposition can be controlled to be lower in parallel (with deposited layers) than on vertical under proper temperature and pressure.   Therefore, the light-receiving layer 314 can be induced to form a prism shape.

[0029]   In addition, in the optical-gate transistor of the invention, a silicone-dioxide layer 410 can be formed first as shown in FIG. 4A.   The silicone-dioxide layer 410 is patterned by a photolithography and etching method to define multiple-gate electrode regions 412.   Afterwards, a source-electrode region 414 and a drain-electrode region 416 are formed by a photolithography and etching method as shown in FIG. 4B.   Subsequently, a prism-shaped, light-receiving layer 418 made of an AIN material is formed by the selective epitaxy mentioned above.   The silicone-dioxide in the gate-electrode regions 412 is etched off to form multiple-gate electrodes 420,

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and then a source electrode 414a and a drain electrode 416a are formed as shown in FIG. 4C.

[0030]   As described above, when an electronic current is generated by illumination on the GaN layer 206, negative bias voltage can be applied to the

5   gate electrodes 420 to increase the intensity of the electronic current. When illumination is stopped, a positive bias voltage can be applied to the gate electrodes 420 so that electrons in the n-type GaN layer are attracted to the gate electrodes to make the conducting channel in the GaN layer 206 disappear, thereby cutting off the electronic current. This avoids a dark

10   current left in a typical optoelectronic device as illumination stops, thereby improving the control efficiency of the optical-gate transistor.

[0031]   Additionally, an AlN layer 422 can also be formed after the gate-electrode regions 412 are formed as shown in FIG. 4D. Subsequently, a source-electrode region 424 and a drain-electrode region 426 are formed by

15   a photolithography and etching method. AlN materials on the gate-electrode regions 412 are then etched as shown in FIG. 4E. Multiple prism-shaped, light-receiving layers 428 are formed by the anisotropic etching method mentioned above. Silicone-dioxide in the gate-electrode regions 412 is etched to form multiple-gate electrodes 430. Lastly, a source electrode 424a

20   and a drain electrode 426a are formed to complete the fabrication of an optical-gate transistor as shown in FIG. 4F.

[0032]   The special features of the optical-gate transistor according to the

invention disclosed above lie in that the GaN-group materials are used for resisting high temperature and high pressure, and a BP buffer layer is used to form better GaN-group layers with a cubic lattice so that a prism-shaped, light-receiving layer can be formed to receive an incident light instead of a

5   gate electrode, thereby improving the sensitivity of the transistor being controlled by illumination.   In addition, the hetero-junction between a doped GaN-group layer and an undoped GaN-group layer is used to generate a high-speed 2DEG, thereby improving the power and performance of the optical-gate transistor.   If gate electrodes are designed in the invention, a

10   dark current inherent to a typical photoelectric device can be further reduced, thereby increasing the efficiency of the optical-gate transistor.

[0033]   While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto.   On the contrary, it is intended to cover various

15   modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.